



<b>Course:</b> Digital Engineering <b>Semester:</b> 1 <sup>st</sup> term 2025/2026.	<b>Lecturers:</b> Dr. Osama Elnahas, Dr. Dina Abdelhafiz, Dr. Bassant Tolba, Dr. Radwa Rady
Tutorial (latch, flip flop, registers, counters)	

Q1. An S-R latch is classified as which type of circuit?

A) Combinational B) Asynchronous sequential C) Synchronous sequential D) Combinational with memory

Answer: B

Why: It stores data (sequential) and does not need a clock (asynchronous).

Key term: Asynchronous → operates without a clock signal.

Q2. An SR latch using NOR gates stores data as long as:

A) Clock is present B) Inputs toggle C) Power is supplied D) Enable is HIGH

Answer: C

Why: Memory is maintained through feedback as long as power exists.

Key term: Feedback → output fed back to input to store state.

Q3. How many stable states does an SR latch have?

A) One B) Two C) Three D) Four

Answer: B

Why: It can store either logic 0 or logic 1.

Key term: Stable state → a condition that remains unchanged.

Q4. An SR latch built with NOR gates uses:

A) Two AND B) Two OR C) Two NOR with feedback D) NAND & NOR

Answer: C

Why: Cross-coupled NOR gates form the latch structure.

Key term: Cross-coupled → outputs connected to opposite inputs.

Q5. For a NOR-based SR latch, when S=0 and R=0:

A) Reset B) Set C) Hold previous state D) Invalid

Answer: C

Why: No input forces change, so memory is preserved.

Key term: Hold state → latch remembers last value.



Q6. Which input causes an invalid state in NOR SR latch?

A) 0,0 B) 0,1 C) 1,0 D) 1,1

Answer: D

Why: Both outputs become 0, breaking complementary rule.

Key term: Invalid state → output is undefined or incorrect.

Q7. Why is S=1 and R=1 invalid?

A) Outputs HIGH B) Outputs LOW C) Oscillation D) Auto reset

Answer: B

Why: NOR gate outputs 0 when any input is 1 → Q and Q' both 0.

Key term: Complementary outputs → Q and Q' must be opposite.

Q8. The feedback path in an SR latch is used to:

A) Increase speed B) Enable clocking C) Store state D) Reduce power

Answer: C

Why: Feedback allows the latch to remember previous output.

Key term: Memory element → circuit that stores data.

Q9. Which operation sets Q = 1 (NOR SR latch)?

A) S=0,R=1 B) S=1,R=0 C) S=0,R=0 D) S=1,R=1

Answer: B

Why: Set input forces output high.

Key term: Set → force Q to 1.

Q10. Which operation resets Q = 0?

A) 1,0 B) 0,0 C) 0,1 D) 1,1

Answer: C

Why: Reset input forces output low.

Key term: Reset → force Q to 0.

Q11. The D latch was introduced mainly to eliminate:

A) Clock dependency B) Feedback C) Invalid state D) Storage

Answer: C

Why: It prevents S and R from being active together.

Key term: D (Data) latch → single input latch.



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Q12. A D latch stores data when:

A) Clock edge B) Enable HIGH C) Enable LOW D) Reset active

Answer: B

Why: It is level-triggered by Enable.

Key term: Level-triggered → active while signal is HIGH.

Q13. A D latch is derived from:

A) JK B) T C) SR D) Master-slave

Answer: C

Why: D latch is a modified SR latch.

Key term: Derived → built from.

Q14. When Enable is LOW, D latch output:

A) 0 B) 1 C) Follows D D) Holds value

Answer: D

Why: No update occurs when Enable is inactive.

Key term: Hold mode → output unchanged.

Q15. Main difference: latch vs flip-flop:

A) Level-triggered B) Async C) Edge-triggered D) No feedback

Answer: C

Why: Flip-flops respond only at clock edges.

Key term: Edge-triggered → changes at rising/falling edge.

Q16. Which requires a clock signal?

A) SR latch B) D latch C) Flip-flop D) MUX

Answer: C

Why: Flip-flops are synchronous devices.

Key term: Synchronous → controlled by clock.

Q17. A D flip-flop stores data on:

A) Input change B) Enable C) Clock edge D) Reset

Answer: C

Why: Storage occurs at clock transition only.

Key term: Clock edge → 0→1 or 1→0 transition.



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Q18. A D flip-flop is constructed using:

A) Two SR B) Two D latches C) NOR only D) XOR

Answer: B

Why: Master-slave configuration of D latches.

Key term: Master-slave → two-stage control.

Q19. In a D flip-flop, Q changes when:

A) D changes B) Clock level C) Clock edge D) Reset inactive

Answer: C

Why: Edge-triggered behavior.

Q20. A shift register is used to:

A) Add numbers B) Store & shift bits C) Decode D) Control memory

Answer: B

Why: Data moves bit-by-bit with clock.

Key term: Shift register → serial data storage.

Q21. Bits stored in shift register equal:

A) Gates B) Latches C) Flip-flops D) Clocks

Answer: C

Why: Each flip-flop stores one bit.

Q22. Data movement in shift register occurs on:

A) Enable B) Clock pulse C) Reset D) Power

Answer: B

Why: Clock synchronizes shifting.

Q23. Shift register can be used as:

A) Frequency divider B) Parallel-serial C) Serial-parallel D) All

Answer: D

Why: It supports all listed functions.

Q24. When  $J=1$  and  $K=1$  (JK flip-flop):

A) Set B) Reset C) Toggle D) Hold

Answer: C

Why: Output switches state each clock.

Key term: Toggle → invert output.



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Q25. JK flip-flop avoids which SR problem?

A) Memory loss B) Invalid state C) Clock need D) Delay

Answer: B

Why:  $J=K=1$  is valid and toggles output.

Q26. A binary counter is built using:

A) Latches B) Gates C) Flip-flops D) Registers

Answer: C

Why: Flip-flops store count bits.

Q27. Each flip-flop represents:

A) Digit B) Bit C) Byte D) Register

Answer: B

Why: One flip-flop stores one bit.

Q28. Binary counters increment on:

A) Enable B) Reset C) Clock pulse D) Data

Answer: C

Why: Clock drives counting sequence.

Q29. Binary counter can act as:

A) Decoder B) Frequency divider C) Generator D) All

Answer: D

Why: Counters support all listed roles.

Q30. Binary counters are commonly used in:

A) Digital clocks B) Error detection C) Timing circuits D) All

Answer: D

Why: All applications rely on counting pulses.